AMENDMENTS TO THE CLAIMS

1. (Canceled)

2. (Currently amended): ~~The method as claimed in claim 1, step F) comprising the following steps:~~A method for fabricating a first contact hole plane in a memory module with an arrangement of memory cells each having a selection transistor, comprising:

A) providing a semiconductor substrate with an arrangement of mutually adjacent gate electrode tracks on a surface of the semiconductor;

B) producing an insulator layer on the semiconductor surface;

C) forming a sacrificial layer on the insulator layer, where regions between the mutually adjacent gate electrode tracks are essentially filled and the gate electrode tracks are covered;

D) forming material plugs on the sacrificial layer for defining a first set of contact openings between the mutually adjacent gate electrode tracks;

E) anistropically etching the sacrificial layer, where the material plugs with the underlying sacrificial layer blocks;

F) producing a vitreous layer with uncovering of the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks, where the regions between the mutually adjacent gate electrode tracks are essentially filled and an essentially planar surface is formed, wherein step F comprises the following steps F1-F6:

F1) removing the material plugs;

F2) removing the uncovered insulator layer on the semiconductor surface between a second set of mutually adjacent gate electrode tracks;

F3) producing dopings in predetermined regions of the uncovered semiconductor surface between the mutually adjacent gate electrode tracks for forming the selection transistors;

F4) producing a liner layer, which includes silicon nitride;

F5) forming the vitreous layer on the liner layer, the regions between the mutually adjacent gate electrode tracks essentially being filled; and

F6) planarizing the vitreous layer with uncovering of the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks, thereby forming the essentially planar surface;

G) etching sacrificial layer material from the vitreous layer for removing the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks;

H) removing the uncovered insulator layer above the first set of contact openings on the semiconductor surface between the mutually adjacent gate electrode tracks; and

I) filling the contact opening regions with a conductive material, in the process forming an essentially planar surface with the surrounding vitreous layer.

3. (Previously presented): The method as claimed in claim 2, wherein the liner layer is a silicon nitride layer or a silicon oxide-nitride layer.

4. (Previously presented): The method as claimed in claim 2, wherein the planarization in method step F6) is effected by chemical mechanical polishing and the end point of the polishing operation being defined at the establishment of a material removal of the liner layer.

5. (Currently amended): The method as claimed in claim ~~1~~2, wherein the vitreous layer formed in method step F) is a BPSG layer.

6. (Currently amended): The method as claimed in claim ~~1~~2, wherein method step C) comprises:

C1) depositing a first sacrificial layer on the insulator layer, the regions between the mutually adjacent gate electrode tracks essentially being filled and the gate electrode tracks being covered;

C2) planarizing the first sacrificial layer with uncovering of the gate electrode tracks, an essentially planar surface being formed; and

C3) depositing a second sacrificial layer.

7. (Previously presented): The method as claimed in claim 6, wherein the second sacrificial layer has a layer thickness of 200 nm to 1000 nm.

8. (Currently amended): The method as claimed in claim ~~1~~2, wherein step C) comprises:
C1') depositing the sacrificial layer on the insulator layer, where the regions between the mutually adjacent gate electrode tracks are filled and the gate electrode tracks are covered; and
C2') planarizing the sacrificial layer, where the gate electrode tracks remain covered and an essentially planar surface is formed.

9. (Previously presented): The method as claimed in claim 8, wherein the sacrificial layer a layer thickness of 200 nm to 1000 nm above the gate electrode tracks.

10. (Currently amended): The method as claimed in claim ~~1~~2, wherein the insulator layer is a silicon dioxide layer.

11. (Currently amended): The method as claimed in claim ~~1~~2, wherein step D) comprises:
D1) depositing a resist layer;
D2) exposing the resist layer by a mask which defines the contact openings between the mutually adjacent gate electrode tracks; and
D3) developing the resist layer to remove the exposed regions of the resist layer and to form the material plugs made from resist material on the sacrificial layer for defining contact openings between the mutually adjacent gate electrode tracks.

12. (Previously presented): The method as claimed in claim 11, wherein an ARC layer is applied on the sacrificial layer before the resist layer.

13. (Currently amended): ~~The method as claimed in claim 1, wherein step D) comprises:~~A method for fabricating a first contact hole plane in a memory module with an arrangement of memory cells each having a selection transistor, comprising:

A) providing a semiconductor substrate with an arrangement of mutually adjacent gate electrode tracks on a surface of the semiconductor;

B) producing an insulator layer on the semiconductor surface;

C) forming a sacrificial layer on the insulator layer, where regions between the mutually adjacent gate electrode tracks are essentially filled and the gate electrode tracks are covered;

D) forming material plugs on the sacrificial layer for defining contact openings between the mutually adjacent gate electrode tracks, wherein step D comprises the following steps D1'-D8':

D1') depositing a hard mask layer on the sacrificial layer;

D2') depositing a resist layer on the hard mask layer;

D3') exposing the resist layer by a mask which defines the contact openings between the mutually adjacent gate electrode tracks;

D4') developing the resist layer to remove the exposed regions of the resist layer outside the contact openings between the mutually adjacent gate electrode tracks;

D5') anistropically etching the hard mask layer with the patterned resist layer as a mask; and

D8') removing the residual resist layer;

E) anistropically etching the sacrificial layer, where the material plugs with the underlying sacrificial layer blocks;

F) producing a vitreous layer with uncovering of the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks, where the regions between the mutually adjacent gate electrode tracks are essentially filled and an essentially planar surface is formed;

G) etching sacrificial layer material from the vitreous layer for removing the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks;

H) removing the uncovered insulator layer above the contact openings on the semiconductor surface between the mutually adjacent gate electrode tracks; and

I) filling the contact opening regions with a conductive material, in the process forming an essentially planar surface with the surrounding vitreous layer.

14. (Currently amended): ~~The method as claimed in claim 1, wherein step D) comprises:~~A method for fabricating a first contact hole plane in a memory module with an arrangement of memory cells each having a selection transistor, comprising:

A) providing a semiconductor substrate with an arrangement of mutually adjacent gate electrode tracks on a surface of the semiconductor;

B) producing an insulator layer on the semiconductor surface;

C) forming a sacrificial layer on the insulator layer, where regions between the mutually adjacent gate electrode tracks are essentially filled and the gate electrode tracks are covered;

D) forming material plugs on the sacrificial layer for defining contact openings between the mutually adjacent gate electrode tracks, wherein step D comprises the following steps D1''-D9'':

D1'') forming a hard mask layer on the sacrificial layer;

D2'') planarizing the hard mask layer;

D3'') depositing a resist layer on the hard mask layer;

D4'') exposing the resist layer by a mask which defines the contact openings between the mutually adjacent gate electrode tracks;

D5'') developing the resist layer in order to remove the exposed regions of the resist layer and to uncover the hard mask layer;

D6'') anistropically etching of the hard mask layer with the patterned resist layer as a mask;

D7'') removing the patterned resist layer;

D8'') introducing a filling material into the etching openings in the hard mask layer; and

D9'') removing the hard mask layer to form the material plugs made from the filling material on the sacrificial layer for defining contact openings between the mutually adjacent gate electrode tracks;

E) anistropically etching the sacrificial layer, where the material plugs with the underlying sacrificial layer blocks;

F) producing a vitreous layer with uncovering of the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks, where the regions between the

mutually adjacent gate electrode tracks are essentially filled and an essentially planar surface is formed;

G) etching sacrificial layer material from the vitreous layer for removing the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks;

H) removing the uncovered insulator layer above the contact openings on the semiconductor surface between the mutually adjacent gate electrode tracks; and

I) filling the contact opening regions with a conductive material, in the process forming an essentially planar surface with the surrounding vitreous layer.

15. (Previously presented): The method as claimed in claim 14, wherein the hard mask layer is a BPSG layer, and the filling material is an organic ARC material.

16. (Currently amended): The method as claimed in claim ~~1~~13, wherein the sacrificial layer is a polysilicon layer.

17. (Currently amended): The method as claimed in claim ~~1~~13, wherein the sacrificial layer is a carbon layer.

18. (Previously presented): The method as claimed in claim 17, wherein a dielectric hard mask layer is additionally provided on the carbon layer.

19. (Previously presented): A method for fabricating a first contact hole plane in a memory module with an arrangement of memory cells each having a selection transistor, comprising:

A) providing a semiconductor substrate with an arrangement of mutually adjacent gate electrode tracks on a surface of the semiconductor;

B) producing an insulator layer on the semiconductor surface;

C) forming a sacrificial layer on the insulator layer, the regions between the mutually adjacent gate electrode tracks essentially being filled and the gate electrode tracks being covered;

D) forming material plugs on the sacrificial layer for defining contact openings between the mutually adjacent gate electrode tracks;

E) anistropically etching of the sacrificial layer, the material plugs with the underlying sacrificial layer blocks remaining;

F) producing a vitreous layer with uncovering of the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks, the regions between the mutually adjacent gate electrode tracks essentially being filled and an essentially planar surface being formed;

G) etching sacrificial layer material from the vitreous layer for removing the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks;

H) removing the uncovered insulator layer above the contact openings on the semiconductor surface between the mutually adjacent gate electrode tracks; and

I) filling the contact opening regions with a conductive material, in the process forming an essentially planar surface with the surrounding vitreous layer,

wherein

step C) comprises:

C1') depositing a first sacrificial layer on the insulator layer, the regions between the mutually adjacent gate electrode tracks essentially being filled and the gate electrode tracks being covered;

C2') planarizing the first sacrificial layer with uncovering of the gate electrode tracks, an essentially planar surface being formed; and

C3') depositing a second sacrificial layer.

20. (Original) The method as claimed in claim 19, wherein the second sacrificial layer has a layer thickness of 200 nm to 1000 nm.

21. (Previously presented): A method for fabricating a first contact hole plane in a memory module with an arrangement of memory cells each having a selection transistor, comprising:

A) providing a semiconductor substrate with an arrangement of mutually adjacent gate electrode tracks a surface of the semiconductor;

B) producing an insulator layer on the semiconductor surface;

C) forming a sacrificial layer on the insulator layer, the regions between the mutually adjacent gate electrode tracks essentially being filled and the gate electrode tracks being covered;

D) forming material plugs on the sacrificial layer for defining contact openings between the mutually adjacent gate electrode tracks;

E) anistropically etching of the sacrificial layer, the material plugs with the underlying sacrificial layer blocks remaining;

F) producing a vitreous layer with uncovering of the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks, the regions between the mutually adjacent gate electrode tracks essentially being filled and an essentially planar surface being formed;

G) etching sacrificial layer material from the vitreous layer for removing the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks;

H) removing the uncovered insulator layer above the contact openings on the semiconductor surface between the mutually adjacent gate electrode tracks; and

I) filling the contact opening regions with a conductive material, in the process forming an essentially planar surface with the surrounding vitreous layer,

wherein

step C) comprises:

C1'') forming a plane first sacrificial layer on the insulator layer, the regions between the mutually adjacent gate electrode tracks essentially being filled and the gate electrode tracks being covered; and

C3'') depositing a hard mask layer formed as a second sacrificial layer.

22. (Previously presented): The method as claimed in claim 19, wherein step D) comprises:

D1') depositing a resist layer;

D2') exposing the resist layer by a mask which defines the contact openings between the mutually adjacent gate electrode tracks; and

D3) developing the resist layer to remove the exposed regions of the resist layer and to form the material plugs made from resist material on the sacrificial layer for defining contact openings between the mutually adjacent gate electrode tracks.

23. (Original) The method as claimed in claim 22, wherein an ARC layer is applied on the sacrificial layer before the resist layer.

24. (Previously presented): A method for fabricating a first contact hole plane in a memory module with an arrangement of memory cells each having a selection transistor, comprising the following method steps:

A) providing a semiconductor substrate with an arrangement of mutually adjacent gate electrode tracks on a surface semiconductor;

B) producing an insulator layer on the semiconductor surface;

C) forming a sacrificial layer on the insulator layer, the regions between the mutually adjacent gate electrode tracks essentially being filled and the gate electrode tracks being covered;

D) forming material plugs on the sacrificial layer for defining contact openings between the mutually adjacent gate electrode tracks;

E) anistropically etching the sacrificial layer, the material plugs with the underlying sacrificial layer blocks remaining;

F) producing a vitreous layer with uncovering of the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks, the regions between the mutually adjacent gate electrode tracks essentially being filled and an essentially planar surface being formed;

G) etching sacrificial layer material from the vitreous layer for removing the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks;

H) removing the uncovered insulator layer above the contact openings on the semiconductor surface between the mutually adjacent gate electrode tracks; and

I) filling the contact opening regions with a conductive material, in the process forming an essentially planar surface with the surrounding vitreous layer,

wherein

step D) comprises:

D1'') forming a hard mask layer on the sacrificial layer;

D2'') planarizing the hard mask layer;

D3'') depositing a resist layer on the hard mask layer;

D4'') exposing the resist layer by a mask which defines the contact openings between the mutually adjacent gate electrode tracks;

D5'') developing the resist layer to remove the exposed regions of the resist layer and to uncover the hard mask layer;

D6'') anistropically etching of the hard mask layer with the patterned resist layer as a mask;

D7'') removing the patterned resist layer;

D8'') introducing a filling material into the etching openings in the hard mask layer; and

D9'') removing the hard mask layer in order to form the material plugs made from the filling material on the sacrificial layer for the purpose of defining contact openings between the mutually adjacent gate electrode tracks.

25. (Previously presented): The method as claimed in claim 24, wherein the hard mask layer is a BPSG layer, and the filling material is an organic ARC material.

26. (Previously presented): The method as claimed in claim 19, wherein the insulator layer is a silicon dioxide layer.

27. (Previously presented): The method as claimed in claim 19, wherein step F) comprises:

F1) removing the material plugs;

F2) removing the uncovered insulator layer on the semiconductor surface between the mutually adjacent gate electrode tracks;

F3) producing dopings in predetermined regions of the uncovered semiconductor surface between the mutually adjacent gate electrode tracks for forming the selection transistors;

F4) producing a liner layer;

F5) forming the vitreous layer on the liner layer, the regions between the mutually adjacent gate electrode tracks essentially being filled; and

F6) planarizing the vitreous layer with uncovering of the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks, the essentially planar surface being formed.

28. (Previously presented): The method as claimed in claim 27, wherein the liner layer is a silicon nitride layer or a silicon oxide-nitride layer.

29. (Previously presented): The method as claimed in claim 27, wherein the planarization in step F6) is effected by chemical mechanical polishing and an end point of the polishing operation is defined at the establishment of a material removal of the liner layer.

30. (Previously presented): The method as claimed in claim 19, the vitreous layer formed in step F) being a BPSG layer.

Add the following new claims 31 and 32:

31. (New): The method as claimed in claim 14, wherein the sacrificial layer is a polysilicon layer.

32. (New): The method as claimed in claim 14, wherein the sacrificial layer is a carbon layer.